



S/N 09/945,507

PATENT

Applicant: Leonard Forbes et al.  
Serial No.: 09/945,507  
Filed: August 30, 2001  
Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE  
Commissioner for Patents  
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Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/075484	February 12, 2002	1303.043US1	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS  
Serial Number: 09/945,507  
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Dkt: 1303.014US1

10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

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Date

9 June '04

By

Timothy B. Clise  
Reg. No. 40,957



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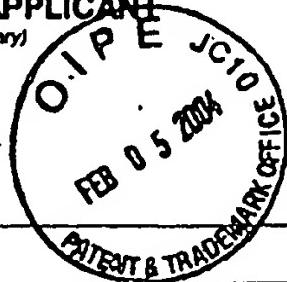
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Substitute for form 1448A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)		Complete if Known	
		Application Number	09/945,507
		Filing Date	August 30, 2001
		First Named Inventor	Forbes, Leonard
		Group Art Unit	2824
		Examiner Name	Dinh, Son
Sheet 1 of 3		Attorney Docket No: 1303.014US1	



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		Application Number	09/945,507
		Filing Date	August 30, 2001
		First Named Inventor	Forbes, Leonard
		Group Art Unit	2824
		Examiner Name	Dinh, Son
Sheet 2 of 3		Attorney Docket No: 1303.014US1	

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## OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>3</sup>
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DATE CONSIDERED 3/5/14

Substitute Disclosure Statement Form (PTO-1449)

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PTO-903A(10-01)

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		Group Art Unit	2824
		Examiner Name	Dinh, Son
Sheet 3 of 3		Attorney Docket No: 1303.014US1	

## OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

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SD	*	Deposition", Electron Devices Meeting, 2000. IEDM Technical Digest. International, (2000),19-22	

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